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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/050,113	Applicant(s) EMA, TAIJI	
	Examiner Matthew E. Warren	Art Unit 2815	

-- The MAILING DATE of this communication app ars on the cov r sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,12,14 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4,12 and 14* is/are allowed.

6)☒ Claim(s) *2,3,5-8 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the RCE filed on September 22, 2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2, 3, and 5-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended limitations of the claims state that the first insulation film is formed "on a rest part of the region...". The specification does not disclose what is the "rest part" of the region between the adjacent conductor patterns. Therefore it cannot be determined what the "rest part" of the region is.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani et al. (US 5,977,583) in view of Kimura (US 6,127,734).

Hosotani et al. shows (figs. 6, 13, 16) a base substrate (11), a first conducting film (15) formed over the base substrate and including a plurality (19) of conductor patterns adjacent to each other, and an etching stopper film (17) covering an upper surface of the conductor patterns. A contact hole is located in a part of a region (where poly 25 fills the hole) between the adjacent conductor patterns and having an end defined by the conductor patterns. A first insulation film (22) fills spaces between the conductor patterns where the contact hole is not formed and does not extend over the etching stopper film. A sidewall insulation film (21) is formed on an inner wall of the contact holes so that side walls of the conductor pattern and the etching stopper film are covered and surrounded (when viewed from above). Hosotani shows all of the elements of the claims except the first insulation film being in contact with the side walls of the conductor patterns and filling spaces between the conductor patterns. Kimura shows (fig. 1) a semiconductor device in which conductor patterns (7) are formed on a substrate (1). A first interlayer insulating film (11) is formed on the substrate and is in contact with the side walls of the conductor patterns. In the configuration of an interlayer insulating film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration (col. 5, lines 50-56). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Hosotani by forming

the first interlayer insulation film on the sidewalls of the conductor patterns as taught by Kimura to simplify the manufacturing process and increase the degree of integration

In re claim 3, Hosotani et al. shows (fig. 6) plurality of contact holes are formed adjacent to each other with the conductor patterns therebetween.

In re claim 7, Hosotani et al. shows (fig. 16) a second conducting film (28) is formed on the first insulation film and connected to the base substrate in the contact hole. The etching stopper film is formed only in a region where the first conducting film intersects the second conducting film.

In re claim 8, Hosotani et al. discloses that the sidewall insulation film is formed of a silicon nitride which has etching characteristics equal to those of the etching stopper film because the etching stopper film is also made of silicon nitride (col. 8, lines 20-46).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani et al. (US 5,977,583) in view of Kimura (US 6,127,734) as applied to claim 2 above, and further in view of Fukase (US 5,728,596).

In re claims 5 and 6, Hosotani et al. in view of Kimura show all of the elements of the claims except the second insulation film on the conductor pattern. Fukase shows (figs. 2A and 2G) a second insulation film (6) of silicon oxide, which is known to have a lower dielectric constant than the silicon nitride etch stop layer (7), formed between the first conducting film and the etching stopper film. It is known in the art that an etching stopper could also be formed of a conducting film because it is well known in the art that

a conductive film, such as metal would have a different etch selectivity as opposed to an insulator such as oxide. The second insulation film is provided as a buffer between the etching stopper and the first conducting film (col. 5, lines 43-54). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate of Hosotani and Kimura by adding an oxide layer between the etching stopper layer and the first conducting film to provide a buffer between them.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukase (US 5,728,596) in view of Kimura (US 6,127,734).

Fukase shows (figure 2G) a semiconductor device in which a first conducting film (4a) of a gate electrode formed on a substrate and having two conductor patterns adjacent to each other. An etch stop layer of silicon nitride (7) is formed on the gate electrode two cover the two patters. A first insulating film (13) is formed over the etch stop layer and a contact hole (15) is formed in the insulating film between the two gate structures. The hole reaches the base substrate and an end of the hole is positioned on the etching stopper film. First and second sidewall insulation films (17' and 17) are formed on an inner wall of the insulation film, on the side of the gate conductor patterns (4a and 4), and on each side of the etch stopper film in the contact hole. The end of the contact hole is defined by four sides including a first pair of sides which are opposed to each other (sides of the gate) and a second pair of sides which are opposed to each other (sides of the insulation film on top of the etch stop film). The first pair of sides is defined by the conductor patterns and the second pair of sides is defined by the first

insulation film. Fukase shows all of the elements of the claims except the first insulation film being in contact with the side walls of the conductor patterns. Kimura shows (fig. 1) a semiconductor device in which conductor patterns (7) are formed on a substrate (1). A first interlayer insulating film (11) is formed on the substrate and is in contact with the side walls of the conductor patterns. The sidewall insulation film is not formed between the sidewalls of the conductor patters and the first insulation film. In the configuration of an interlayer insulating film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration (col. 5, lines 50-56). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of Fukase by forming the first interlayer insulation film on the sidewalls of the conductor patterns as taught by Kimura to simplify the manufacturing process and increase the degree of integration.

Allowable Subject Matter

Claims 1, 4, 12 and 14 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art references do not show a sidewall insulation film formed on inner walls of the first insulation film, each sidewall of the two conductor patterns, and each side wall of the etching stopper film in the contact hole wherein each of the etching stopper films is completely covered by the first insulation film and the respective sidewall insulation films. The prior art also does not show a plurality of bit lines formed over the first insulation film and extended in a second direction, an etching stopper film covering

upper surfaces of the bit lines and a second insulation film filling spaces between the plurality of bit lines where the contact hole is not formed, wherein the second insulation film does not extend over the etching stopper film.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed with respect to claims 2 and 36 have been fully considered but they are not persuasive. The applicant primarily argues that Kimura cannot be combined with Hosotani or Fukase due to process limitations that restrict removal of sidewall spacers. The examiner believes that Kimura can be combined with the primary references of Hosotani and Fukase because those processes are irrelevant to the final structure of the device. In Hosotani, the sidewall spacers (21) are not necessary between the adjacent conductors where the insulating layer (22) is formed. The is no need for protection because there is no conductive material between the adjacent conductors. In Fukase, a spacer is not particularly needed for the middle conductor pattern (4a) in figure (2G) because there are no LDD regions next to the gate. Therefore the application of spacers for that conductor pattern is a non critical step. Furthermore, as explained in Kimura, if one were to increase the degree of integration or reduce manufacturing steps, one of ordinary skill in the art would not form the

spacers on the side of the conductor where there is no contact hole formed. Therefore, Kimura, which shows benefits of forming an insulation film between adjacent conductors without spacers, can be combined with Hosotani and Fukase to disclose all the limitations of the instant invention. For these reasons, the 103 rejection above is still proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew E. Warren
October 1, 2003